IN THE CLAIMS:

Listing of claims:

1. (previously presented) A method for manufacturing a semiconductor chip, the method comprising forming a multi-layer electrode on a first surface of a semiconductor chip, the electrode formed to include a first conducting layer and a second conducting layer formed in direct contact with the first conducting layer, wherein the first conducting layer is positioned between the second conducting layer and the first surface of the semiconductor chip, and then digging a hole from a second surface of the semiconductor chip until the electrode is exposed.

2. (original) A method as in claim 1, wherein the second surface is located opposite to the first surface.

3. (previously presented) A method as in claim 2, wherein the hole contacts the first layer of the electrode and does not contact the second layer of the electrode.

4. (previously presented) A method for manufacturing a semiconductor chip, the method comprising: forming an electrode on a first surface of a first semiconductor chip and thereafter forming a hole from a second surface of the first semiconductor chip until the electrode is exposed, forming a dielectric layer on the second surface of the first semiconductor chip and on the first semiconductor chip in the hole, wherein the dielectric layer has an opening and the electrode is exposed through the opening, forming a protrusion by etching a surface of a second semiconductor chip and thereafter forming an abutting electrode on an apex section of the protrusion, and positioning the first semiconductor chip and the second semiconductor chip such that the abutting electrode is in electrical contact with the electrode through the opening.

5. (previously presented) A method as in claim 4, wherein forming a hole from another surface comprises forming the hole from a surface that is opposite to the surface the electrode was formed on.

6. (previously presented) A method for manufacturing a semiconductor device, the method comprising: forming a metal film on a surface of a first semiconductor chip, forming a hole by an anodic forming method using a dielectric layer coated on an opposite surface of the first semiconductor chip as a mask, thereafter removing the metal film, and forming a multi-layer electrode on a portion of the surface of the first semiconductor chip in a manner to embed the hole.

7. (previously presented) A method for manufacturing a semiconductor device according to claim 2, wherein, after the hole is formed, a metal film is formed on the electrode through the hole.

8. (previously presented) A method for manufacturing a semiconductor device according to claim 3, wherein, after the hole is formed, a metal film is formed on the first layer of the electrode through the hole so that the first layer of the electrode is positioned between the metal film and the second layer of the electrode.

9-22. (canceled)

23. (previously presented) A method for forming a semiconductor device comprising:

forming a first electrode on a first surface of a first substrate;

forming a hole from a second surface of the first substrate to the first surface, wherein a portion of the first electrode is exposed through the hole, wherein the hole is defined by an interior surface of the first substrate and the exposed portion of the first electrode;

forming a second electrode on a second substrate;

forming a dielectric layer on the interior surface of the first substrate, the dielectric layer having an opening therein, and positioning the dielectric layer so that a portion of the first electrode is exposed through the opening; and

positioning the second electrode in the opening and electrically connecting the first electrode to the second electrode through the opening.

24. (previously presented) A method for manufacturing a semiconductor device, comprising:

providing a first substrate comprising a semiconductor chip having a first surface and a second surface opposite the first surface;

forming a first electrode on the first surface of a semiconductor chip, the electrode including a first electrode surface in contact with the semiconductor chip;

removing a portion of the semiconductor chip from the second surface of the semiconductor chip to form a hole extending through the semiconductor chip, the hole being defined by interior sidewalls of the semiconductor chip and an exposed portion of the first electrode;

forming a dielectric layer on the interior sidewalls of the semiconductor chip, wherein the dielectric layer is formed to include an opening and a portion of the first electrode surface is exposed through the opening;

providing a second substrate having an second electrode thereon, the second electrode extending a distance above a first surface of the second substrate; and

positioning the second electrode within the hole and in electrical contact with the first electrode.

25. (previously presented) A method as in claim 24, wherein a portion of the second substrate is positioned within the hole.

26. (previously presented) A method as in claim 24, wherein the second substrate comprises a semiconductor chip and a portion of the semiconductor chip is positioned within the hole.

27. (previously presented) A method as in claim 26, wherein the second electrode is formed on a first surface of the second substrate, further comprising:

forming a conducting lead extending from the second electrode on the first surface of the second substrate; and

forming the dielectric layer on the interior sidewalls to also extend on the second surface of the first substrate.

28. (previously presented) A method as in claim 27, further comprising forming a conducting material within the opening between the first electrode and the second electrode.

29. (previously presented) A method as in claim 27, further comprising forming a metal layer on the first electrode through the opening, prior to the positioning the second electrode within the hole.

30. (previously presented) A method as in claim 24, where the interior sidewalls are formed so that an angle at an intersection of an interior sidewall and the second surface is 90 degrees.

31. (previously presented) A method as in claim 24, where the interior sidewalls are formed so that an angle at an intersection of an interior sidewall and the second surface is 54.74 degrees.

32. (previously presented) A method as in claim 24, wherein the removing a portion of the semiconductor chip from the second surface of the semiconductor chip is carried out using an anisotropic etching technique.

33. (previously presented) A method for manufacturing a semiconductor device, comprising:

providing a first substrate comprising a semiconductor chip having a first surface and a second surface opposite the first surface;

forming a first electrode on the first surface of a semiconductor chip, the electrode including a first electrode surface in contact with the semiconductor chip; wherein the first electrode includes a first layer comprising tungsten and a second layer comprising aluminum, wherein the first electrode surface is part of the first layer;

removing a portion of the semiconductor chip from the second surface of the semiconductor chip to form an opening extending through the semiconductor chip and extending to the first electrode surface, the opening being defined by interior sidewalls of the semiconductor chip and an exposed portion of the first electrode;

providing a second substrate having an second electrode thereon, the second electrode extending a distance above a first surface of the second substrate; and

positioning the second electrode within the opening and in electrical contact with the first electrode.

34. (previously presented) A method for manufacturing a semiconductor device, comprising:

providing a first substrate comprising a semiconductor chip having a first surface and a second surface opposite the first surface;

forming a first electrode comprising platinum on the first surface of a semiconductor chip, the electrode including a first electrode surface in contact with the semiconductor chip;

placing the first substrate into a processing container having a processing electrode and a lamp therein, wherein the first substrate is spaced apart from the processing electrode and the lamp;

forming a patterned dielectric layer so that the second surface includes a masked portion and an exposed portion;

introducing an acid into the container;

irradiating the second surface with the lamp;

applying a voltage between the processing electrode and the first electrode; and

forming an opening that extends through the semiconductor chip through the exposed portion of the second surface.

35. (previously presented) A method as in claim 34, further comprising:

removing the first electrode comprising platinum from the first surface of the semiconductor chip;

forming an aluminum electrode on the first surface of the semiconductor chip that covers the opening;

removing the patterned dielectric layer from the second surface; and

forming a thermal oxide on the second surface.

36. (previously presented) A method as in claim 34, wherein the opening includes sidewalls, and an angle between the sidewalls and the second surface is 90 degrees.

37. (previously presented) A method as in claim 34, further comprising forming the patterned dielectric layer so that the exposed portion of the second surface includes a plurality of exposed regions and the masked portion includes a plurality of masked regions, and the plurality of exposed regions are separated from one another by the masked regions, and wherein a plurality of openings that extend through the semiconductor chip through the exposed regions are formed.

38. (currently amended) A method as in claim 1, wherein the ~~the~~ first conducting layer comprises tungsten, and wherein the first conducting layer is exposed during the digging a hole from a second surface of the semiconductor chip until the electrode is exposed.

39. (previously presented) A method as in claim 38, wherein the second conducting layer comprises aluminum.

40. (new) A method as in claim 6, wherein the forming a hole by an anodic forming method includes providing a container into which the first semiconductor chip is placed, providing an electrode in the container that is not in direct physical contact with the first semiconductor chip, introducing an acid into the container, and applying a voltage between the metal film on the surface of the first semiconductor chip and the electrode in the container.